Chapter 01. Digital to Analog Converter (DAC). Analog to Digital Converters (ADC)

1. The following form of the arithmetic representation of numbers with $n_1 + n_2 + 1$ digits in the numbering base B is considered:

$$N = \pm \sum_{k=-n_2}^{n_1} c_k B^k \quad \text{with digits and base} \quad c_k \in \{0,1,...,B-1\} \text{ si } B \in \mathbb{N}^* - \{1\} \quad (1.1)$$

Questions:

a) Find out the range, precision and the number of numbers for n_1=2, n_2=3 , when B=10 and when B=8

b) Determine the correct "code" with minimum number of digits (n_1 şi n_2) when B=10 and B=8 for the exact representation of the number N=877.1875/7 (in decimal base B=10).

2. Perform the following conversions on the minimum number of digits:

a) Convert the binary number $101101,010101|_B$ into Decimal base (D), Octal (O) and Hexadecimal (H)

b) Convert the decimal number 41.27 into B, O, H bases within a maximum error $e_D \le 0,005$ (in decimal base). What is the minimum necessary number of digits for each conversion?

3. Present the numbers: +0,390625 and –0,390625 into two's complement, into shifted binary code and into modulus-sign

4. Perform the following operations for the binary subunitary numbers represented in two's complement:

a) 6 bits sums: 01010+00101, 11100+11001, 01110+10100.

b) 8 bits products (including the bit of sign): 01011*0101 şi 10101*0101.

Verify the results executing the computations in decimal base.

5. Consider that the quantization samples of a sine voltage with magnitude U_0=0.5 V_{ref} supply the bipolar DAC working according to shifted binary code. Due to an error the bit b_1 (MSb) is short-circuited to the ground. Plot the output signal wave. Which wave form will result if b_1 would be connected to the logic "1" level? Resolve the problem if we consider the same hypothesis only for b_2.

6. We consider the DAC in the fig. 6.

a) Determine the conversion relationship, the resolution and the output voltage range.

b) If the switching time of the electronic switches is 100ns, determine the maximum capacity of the summing node C_n , such that the DA conversion time is smaller than 500ns.

c) Supposing that the MOS switches are used, like the ones in Fig.1.r.b, having the on resistance r_a = 100 Ω and the off resistance r_o=5MΩ, compute the error with respect to 0 and the end scale error.

d) Assuming a resistors tolerance ε_R= 0,1% and a relative voltage error ε_{VR}=0,2%, determine ε_{V0} (relative error of the output voltage) for the hexadecimal input 80H. How is the full-scale voltage affected by the resistors error source?

e) Determine the maximum tolerance of the reference voltage V_r such that the converter will work on 8 bits (ignoring the tolerance of the resistors).

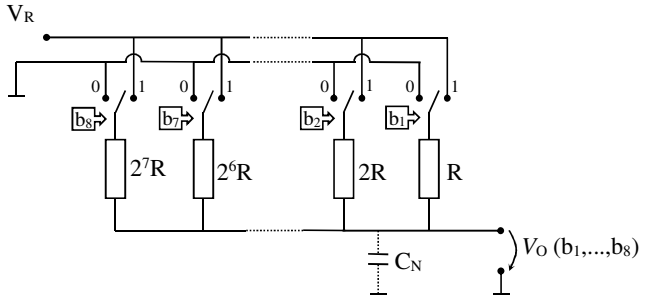


Fig. 6

7. The AD 7520 DAC integrated convertor, with the equivalent schema from the fig. 7. is considered. The electronic switches and the operational amplifier are both ideal, except switching time, of 400ns, and AO slew rate, SR = 10V/μs. Questions:

a) Determine the conversion relationship, the output voltage range and its resolution, if V_R = 5.12V and R = 10kΩ.

b) Compute the absolute error of the output voltage for the hexadecimal number 080H applied at the input, if tolerances for resistances and voltage V_R are known $\varepsilon_R = \varepsilon_{V_R}$ = 0.1%. Compare this error to DAC resolution.

c) Evaluate the maximum relative error ε_{V_R} in order to DAC works on 10 bits, if $\varepsilon_R = 0$.

d) What is the maximum frequency of the sine wave with magnitude U_{01} = 1V and DC component equal to half of magnitude that can be reconstruct by this DAC? But for U_{02} = 3V ?

e) Evaluate the SNR due to quantization process, for (d).

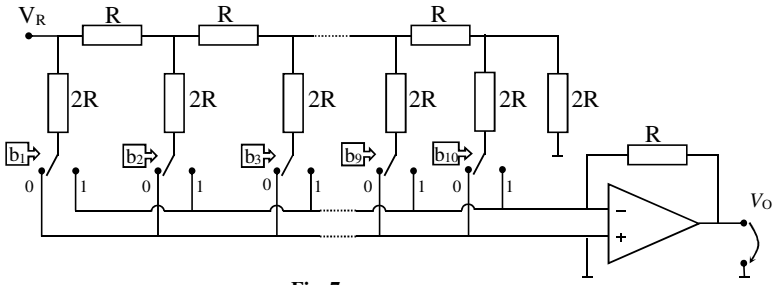


Fig. 7

8. The simplified schema of integrated DAC08 is given in the figure 8. Determine the conversion relationship for the output currents I_0 and I_0'. We consider $\beta >> 20 \rightarrow \alpha \approx 1$ for transistors $T_0 \div T_9$. Also the voltages $V^- < 0V$ and $V_5 > 0V$ are appropriate in order that all BJT transistors are in forward active mode (They are current supplies).

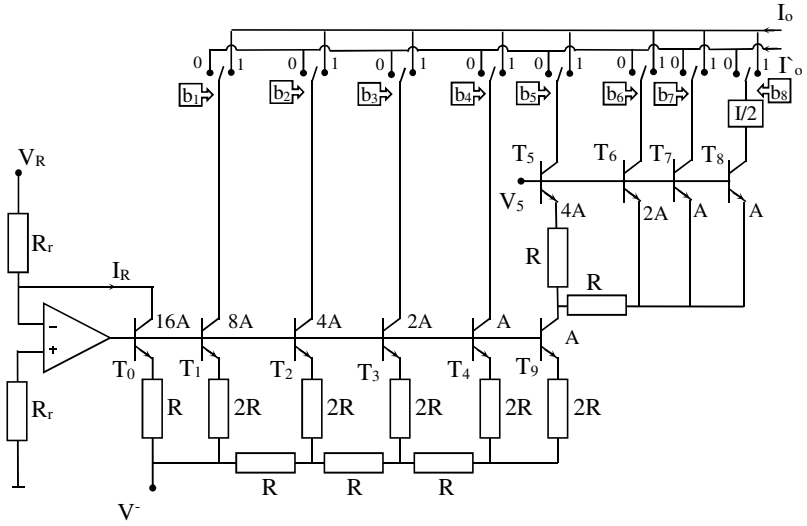


Fig. 8

9. We consider the DAC convertor with voltage output in fig. 9. We know reference voltage V_R= +10.24V ± 20mV; R_r = 5kΩ ± 0,5%, $R_0 = R_1 = R_2$ = 10kΩ ± 0,5%, V_A = +20V ± 10mV. Quiz:

a) Determine the conversion relationship, the output voltage range and DAC resolution.

b) Evaluate the absolute limit error of V_0 for the worst case.

c) The DAC is feed on with samples for triangle wave form, full scale signal. Compute the SNR due to quantization process (assuming adequate filtering).

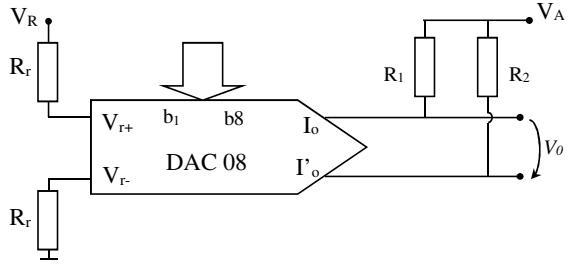


Fig. 9

10. We assume the voltage output DAC convertor in fig. 10. We know reference voltage V_R = +5.12V ± 10mV; R_r = 5kΩ ± 0,5%, R_2 = 10kΩ ± 0,5%. Quiz:

a) Evaluate the value of R_1 in order to be bipolar DAC working with the binary shifted code.

b) Determine the conversion relationship, the output voltage range and DAC resolution.

c) Compute the relative limit error of V_0 for the hexadecimal combination 20H applied to the input.

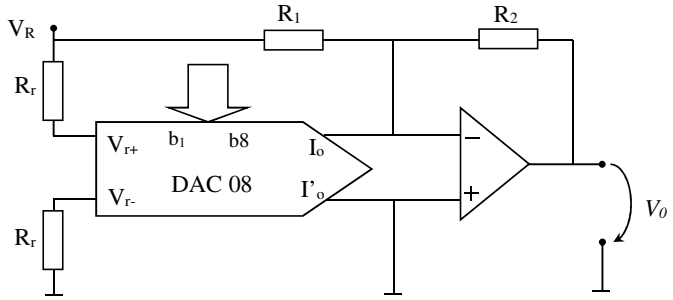


Fig. 10

11. For the voltage output DAC in fig 11 we know V_R = +10.24V ± 20mV; R_r = 5kΩ ± 0,1%, ε_{R1}= ε_{R2} = 0,1% and the absolute limit error of the DAC08 convertor output currents being 0,2%·I_{ref}. Questions:

a) Determine R_1 and R_2 in order to obtain a binary shifted code bipolar DAC, with output range $V_{0\,min}$ = -10.24V şi $V_{0\,max} \approx -V_{0\,min.}$

b) Evaluate absolute limit error of V_0 for the input combination 40H.

c) Knowing that operational amplifier has SR=4V/µs, determine the maximum frequency of full scale sine wave signal that can be recovered from its samples.

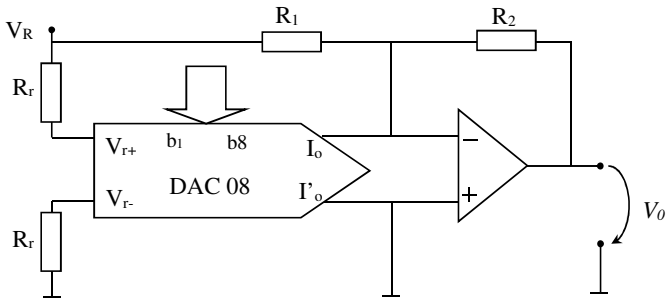


Fig. 11

12. Consider the voltage output DAC in fig.12. We know V_R = +2.56V ± 10mV; R_r = 4kΩ ± 0,5%, R_1 = R_2= 6kΩ ± 0,5%. Quiz:

a) Determine the DAC conversion relationship, the output voltage range and its resolution.

b) Evaluate the relative limit error of V_0 for the combination 20H applied at the input.

c) Plot the DAC output wave form for the numbers N_1=82H for t_1=10µs, N_2=48H for t_2=20µs and N_3=A4H for t_3=10µs periodical supply the DAC input. Determine the mean and root mead squared (rms) of output voltage.

13. Assume that the DAC converter in fig 13 has V_R = +5.12V ± 5mV; R_r = 10kΩ ± 0,5%, R_1 = 5kΩ ± 0,5%. Questions:

a) Determine the DAC conversion relationship, the output voltage range and its resolution.

b) Compute the relative limit error of output voltage V_0 for the input 20H

c) Evaluate the relative limit error of V_0 for worst case.

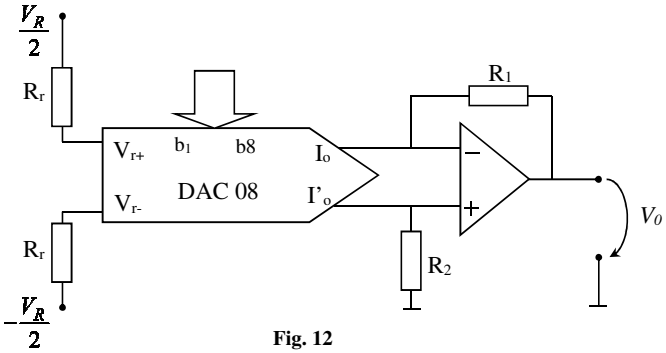


Fig. 12

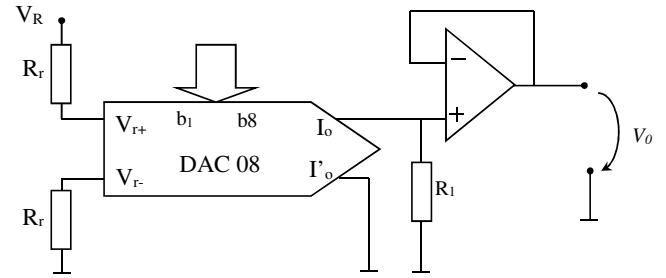


Fig. 13

14. Consider the DAC converter in fig 14, with V_R = +10.24V ± 0,1V; R_r = 10kΩ ± 0,5%, R_1 = 5kΩ ± 0,5%. Questions:

a) Determine the conversion relationship, the output range and convertor resolution.

b) Evaluate the relative limit error of V_0 for the input 24H.

c) Supposing that DAC 08 has the propagation time 35 ns , its output capacity C_0=15pF and the operational amplifier has the input capacity C_{in}=17pF, determine the all conversion time. How can it be reduced?

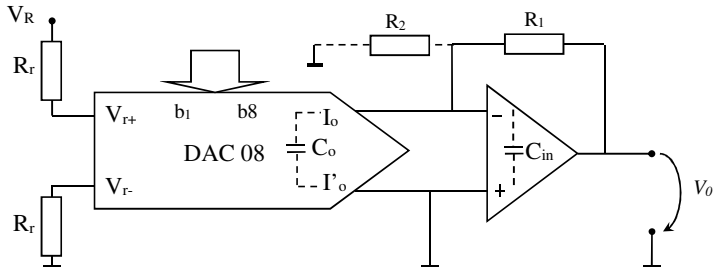


Fig. 14

15. We consider the SAR-ADC (Successive Approximation Register) in fig. 15. SAR works on the rising edge of the clock. It generates the value "1" logic at the output Q_i during "i"-th cycle and at beginning of the next cycle, "i+1", it stores the value from the comparator output D, in Q_i. We know V_R=10,24V±10mV, R_1=R_r=2kΩ , R_2=1,024MΩ, R_3=4kΩ. All the resistances have the tolerance ε_R=0,2%.

a) Determine the conversion relation, the output voltage domain of the converter and its resolution. What type of quantization does the ADC realize?

b) Plot the DAC output current, I_0, during ADC quantization process when U_i = 3V

c) Determine the minimum amplification of the comparator if the minimum voltage for the "D" SAR input is 3V, in order to decide "1" logic.

d) Determine the values for R_3 for which the ADC does the quantization through truncation and ceiling.

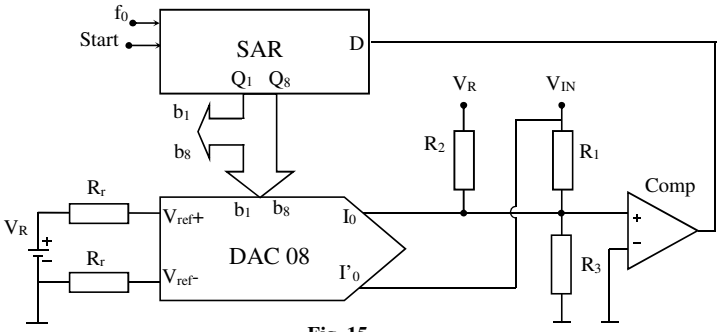


Fig. 15

16. Let be the SAR-ADC in fig. 16. We know V_R=10,24V±10mV, R_1=R_r=4kΩ, R_2, R_3=10kΩ. All the resistances have tolerance ε_R.

a) Determine the conversion relation and the values of R_2 for a bipolar converter a bipolar converter with rounding, truncating and ceiling quantization.

b) Evaluate the maximum value of ε_R for which the converter works properly on 8 bits, for rounding quantization.

c) Determine the quantization SNR (signal to noise ratio) of a triangular symmetric signal with the magnitude U_0 = 4V with the conditions from b).

d) We assume that SAR propagation time is t_{SAR}=100ns, the DAC conversion time is t_{DAC} = 300ns and the comparator has SR = 9V/μs (Slew Rate). Determine the maximum frequency f_{max} of a sine wave signal whose samples may be quantized with this ADC if the minimum voltage for the "D" input in SAR is 3V, in order to decide "1" logic.

e) Evaluate the quantization SNR for the full scale sine wave signal with frequency $1/20\cdot f_{max}$, from (d) .

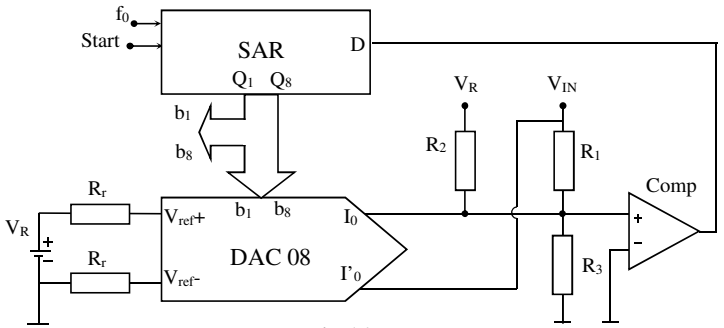


Fig. 16

17. We assume that the SAR-ADC in fig 17is used to measure the voltage from an ideal voltage source. We know: the internal ADC has 10 bits, with voltage output, output resistance R_0 = 10 kΩ and relative error ε_{Udac} = ±2,5×10^{-4}; comparator amplification A = 4×10^3, comparison time t_{comp}≤1μs, input resistance R_{in} = 10kΩ, offset voltage V_{os} = ±5,0 mV. Also the total capacity of the comparison node is C_0 ≤ 20pF and the minimum comparator output voltage V_0 = 3V is necessary to SAR to decide logical "1". Determine:

a) U_{CS} and the number of digits of an electronic voltmeter which might use this ADC if the supplementary error is at most equal with quantization error, and the static error of the comparator to be equal with the dynamic error of the ADC;

b) Minimum ADC conversion time and maximum clock frequency if the conditions from (a) are satisfied;

c) Supposing the input analog signal is not sampled before quantization process and the clock frequency f_{CK} = 400 kHz, evaluate the $\left(\frac{dU_{in}}{dt}\right)_{max}$ at which the output binary sequence for one sample remains "undisturbed".

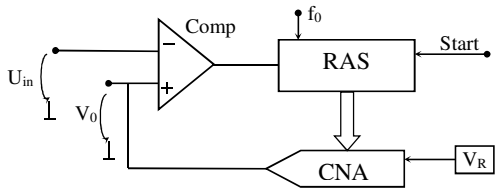


Fig. 17

18. Let be the unipolar ADC with the schema from fig. 18. We know R=2kΩ, V_R = 10,24V The 10 bits DAC has conversion time $t_{DAC} \leq$ 0,5 μs at a dynamic error $\varepsilon_{DAC\_dyn} \leq 0{,}25\ I_{LSB}$. The comparator is an OA (operational amplifier) with $I_b \leq$0,5 μA, $t_{comp} \leq$ 0,5μs at ΔU_{in_OA} = 2,5 mV, and open loop amplifier factor $A \to \infty$. Questions:

a) Evaluate $I_{0\ max}$, $I_{0\ LSB}$ and the maximum clock frequency $f_{ck\ max}$ for $\varepsilon_{ADC\_dyn} < 0{,}25\ V_{LSB}$;

b) Compute maximum signal frequency f_{max} to have anaccurate conversion if the control logic of measurement circuit works in accordance with the tracking algorithm, the clock frequency is maximum, $f_{ck} = f_{ck\_max}$ and the input signal is $u_{in}(t) = 5+5\cdot\sin(2\pi f)$ [V].

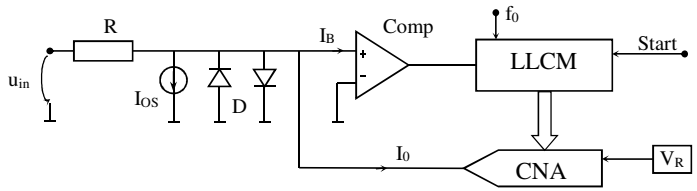


Fig. 18

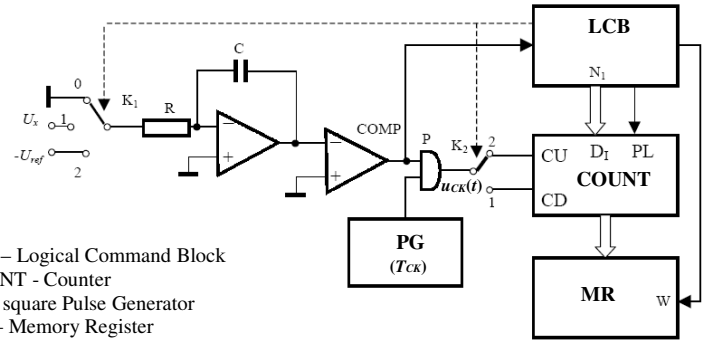
19. We consider the ADC converter with double slope integration from fig. 19. This is the sketch of the corresponding block for the DC voltmeter of digital multimeter with AC electric power supply with (f_{supply}=50Hz). We consider R=10KΩ, U_{ref}= 10V, ε_{Uref} =1‰, ε_R=1%, ε_C=1‰ and ε_{Tck}= 10^{-5}. The counter is BCD with 3 digits having has n_{bits} = 12 bits (3 modules of 4 bits). Questions:

a) Explain the functioning principles of the schema, determine the conversion relationship and represent the chronograms of the voltages $u_C(t)$, $u_{COMP}(t)$, $u_{CK}(t)$

b) Determine the ADC conversion input range, the resolution and the conversion time.

c) Evaluate the relative error of the measurement U_x = 4,5V.

d) Evaluate SRR (the rejection ratio of the serial alternative perturbations) for a sine wave noise signal with the frequency of 112,5 Hz superimposed on the desired signal. Determine the minimum SRR of sine wave perturbation signal with the frequency 5kHz ± 1%.



BLC – Logical Command Block
COUNT - Counter
PG – square Pulse Generator
RM – Memory Register

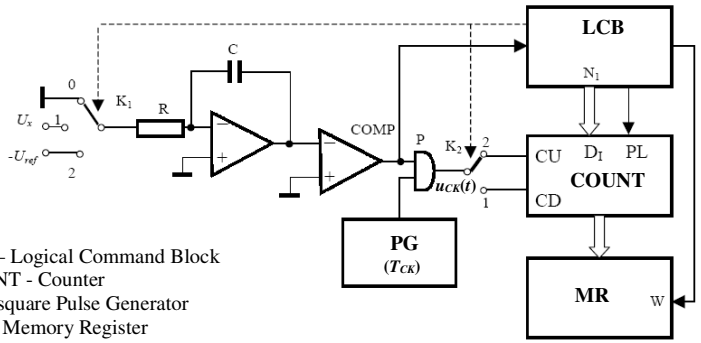
Fig. 19

20. Let be the ADC with double slope integration from fig 20. We know $K = R_1 / R_2$ =1, ε_K = 1‰, U_{ref}= 10V, ε_{Uref} =1‰, ε_R=1% and ε_{Tck}= 10^{-5}. The counter is binary, and it works on 12 bits. Questions:

a) Explain the functioning of the schema, determine the conversion relationship and plot the chronogram for the voltage $u_C(t)$

b) Determine the ADC conversion range, the resolution and the conversion time.

c) Evaluate the relative measuring error for U_x= - 2,5V;



BLC – Logical Command Block
COUNT - Counter
PG – square Pulse Generator
RM – Memory Register

Fig. 20

21. We consider the ADC with linear slope from fig. 21, which works on 9 bits, including the sign bit, with LVG, a linear variable voltage generator, commanded on "0" level. It generates a linear increasing voltage starting from $-U_{fM}$ up to $+U_{fM}$. We know: U_{fM}=2.55V, and clock frequency f_{CK}=10MHz. Questions:

a) Explain the functioning of the schema, determine the conversion relationship and plot the chronogram of the voltages. What code is used for the binary number?

b) Determine the maximum frequency for the sinewave signal whose samples can be converted with this ADC.

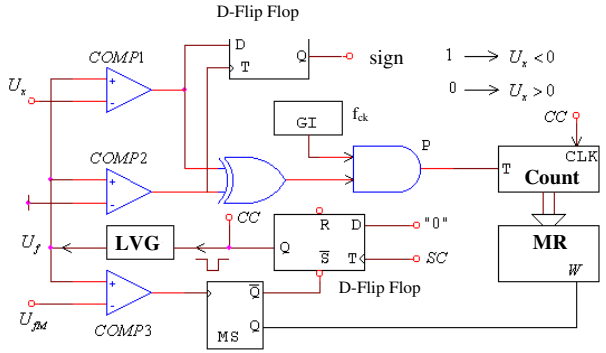


Fig. 21

EMI ADC – DAC Applications